Introduction to CAD tools

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**Introduction**

The purpose of this lab is to learn about the basic CAD tools and how to use Quartus II software to create and simulate block diagram schematics and VHDL based designs. The use of CAD tools can significantly decrease cost as not all circuits have to be built out to test their functionality. Using Quartus II, we can observe the outputs of the circuits created which can help further the learning process about logic gates and using VHDL.

**Results**

Diagram, schematic

Description automatically generated

**Figure 1:** Block diagram schematic of Part 1

Table

Description automatically generated

**Figure 1a:** Desired output of Figure 1

Graphical user interface

Description automatically generated with low confidence

**Figure 2:** Waveform with output waveform of the block diagram schematic in Figure 1

A picture containing diagram

Description automatically generated

**Figure 3:** Block diagram schematic of Part 2 using the symbols created with VHDL

**Analysis**

In Figure 1, the block diagram schematic is built with 2 AND gates, 1 OR gate and 1 NOT gate. This would produce the desired output for this lab which is show in the waveform in Figure 2. The desired output is shown in Figure 1a which corresponds to the resultant output in Figure 2 produced by the circuit. The first part of the lab was to demonstrate the general equation . Since this equation is in its minimal form, the circuit presented in Figure 1 is a direct visualization and implementation of the equation using CAD tools.

Figure 3 shows the 2 symbols that were created from the VHDL. VHDL1 models the equation where VHDL2 models 2 different equations and .